This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

~~19~~14. (Amended) A method of fabricating an integrated circuit, the method comprising:

providing a plurality of inverters as part of said integrated circuit;

providing a plurality of MACROs as part of said integrated circuit;

providing a first layer of metallization;

providing a second layer of metallization;

utilizing no local interconnect in said second layer of metallization to configure said plurality of inverters;

utilizing said second layer of metallization to connect at least two of said MACROs.

~~20~~15. (Amended) The method as described in claim ~~19~~ 14 and further comprising:

utilizing in at least one of said MACROs no local interconnect within said second layer of metallization.

~~21~~16. (Amended) The method as described in claim ~~19~~ 14 and further comprising:

utilizing in a plurality of said MACROs no local interconnect within said second layer of metallization.

~~22~~17. (Amended) The method as described in claim ~~19~~ 14 and further comprising:

utilizing in all of said MACROs no local interconnect within said second layer of metallization.

~~23~~18. (Amended) The method as described in claim ~~19~~ 14 and further comprising;

~~embedded~~ embedding at least one of said MACROs within a standard cell array of said integrated circuit.

~~24~~19. (Amended) The method as described in claim ~~23~~ 14 wherein said standard cell array comprises a row pitch, said method further comprising:

utilizing a MACRO having a row pitch equivalent to said standard cell array.

~~30~~20. (Amended) An integrated circuit, comprising:

a logic inverter comprising:

an n-channel field effect transistor;

a p-channel field effect transistor;

a gate, formed in a layer of polysilicon; and

a drain of the p-channel field effect transistor and a drain of the n-channel field effect transistor formed in said same layer of polysilicon.

~~31~~21. (Amended) The integrated circuit as described in claim ~~30~~20, wherein the polysilicon comprising said gate is coplanar with the polysilicon comprising said drain of the p-channel field effect transistor and said drain of the n-channel field effect transistor.

~~32~~22. (Amended) The integrated circuit as described in claim ~~30~~20, further comprising:

a first layer of metallization; and

a second layer of metallization, wherein the second layer of metallization comprises substantially no local interconnect.

~~33~~23. (Amended) The integrated circuit as described in claim ~~32~~22, wherein said second layer of metallization comprises no local interconnect.

~~34~~24. (Amended) The integrated circuit as described in claim ~~30~~20, further comprising:

a plurality of MACROs;

a fist layer of metallization; and

a second layer of metallization interconnecting said plurality of MACROs.

~~35~~25. (Amended) The integrated circuit as described in claim ~~30~~24, further comprising:

a trace, formed in said layer of polysilicon, wherein said trace connects said drain of said p-channel field effect transistor and said drain of said n-channel field effect transistor.

~~36~~26. (Amended) The integrated circuit as described in claim ~~35~~24, further comprising, no local interconnect within said second layer of metallization in at least one of said MACROs.

~~37~~27. (Amended) The integrated circuit as described in claim ~~35~~24, further comprising, no local interconnect within said second layer of metallization in a plurality of said MACROs.

~~38~~28. (Amended) The integrated circuit as described in claim ~~35~~24, further comprising, no local interconnect within said second layer of metallization in all of said plurality of MACROs.

~~39~~29. (Amended) The integrated circuit as described in claim ~~35~~24, wherein at least one of said MACROs is comprised by a standard cell array of the integrated circuit.

~~40~~30. (Amended) The integrated circuit as described in claim ~~39~~29, wherein said standard cell array comprises a row pitch and at least one MACRO has a row pitch equivalent to the row pitch of said standard cell array.